Si Microwire Solar Cells: Improved Efficiency with a Conformal SiO_2 Layer

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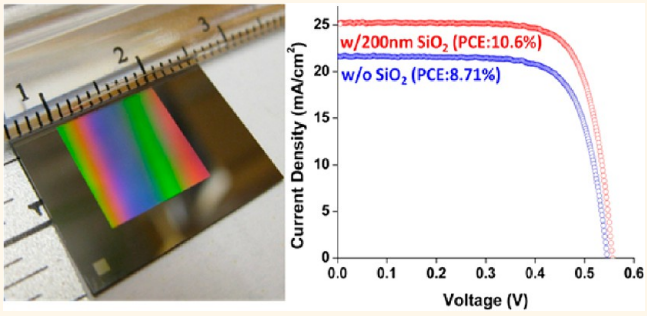
ABSTRACT Silicon microwire arrays have attracted considerable attention recently due to the opportunity they present as highly efficient and cost-effective solar cells. In this study, we report on efficient Si microwire array solar cells with areas of 1 cm^2 and Air Mass 1.5 Global conversion efficiencies of up to 10.6%. These solar cells show an open-circuit voltage of 0.56 V, a short-circuit current density of 25.2 mA/cm^2, and a fill factor of 75.2%, with a silicon absorption region that is only 25 μm thick. In particular, the maximum overall efficiency of the champion device is improved from 8.71% to 10.6% by conformally coating the wires with a 200 nm thick SiO_2 layer. Optical measurements reveal that the layer reduces reflection significantly over the entire visible range.



KEYWORDS: silicon · microwire · solar cells · radial junction · antireflection · light trapping

The nano- and microstructuring of Si surfaces has been extensively investigated as a means for developing highly efficient and low cost solar cells. Structured patterning of a planar Si surface leads to broadband antireflection as well as enhanced light trapping efficiency.[1−7] These features in turn enable solar cells based on ultrathin layers, thereby greatly reducing fabrication costs. Recently, a theoretical study predicted that optimally structured nanocones enable 10 μm thick Si solar cells to achieve short-circuit current densities up to 39.1 mA/cm^2.[8] Among the various surface structures possible, wire arrays with radial p−n junctions formed by core−shell structures are particularly attractive, as the functions of light absorption and carrier collection become decoupled as they occur along orthogonal directions.[9−12] In other words, incident light is absorbed along the long wire axis, while generated charge carriers can be collected along the relatively short radial direction. Decreasing the path length of the minority carriers in this way offers the possibility of using low grade materials by minimizing carrier recombination.[13]

Despite the favorable features that they offer, solar cells based on wire arrays have thus far exhibited efficiencies that are very modest in comparison to their planar counterparts. Most of previously reported Si nanowire based solar cells[14−16] exhibited efficiencies below 5%, while conventional planar Si solar cells can show efficiencies exceeding 20%.[17,18] In addition, these nanowire solar cells were generally smaller than 0.1 cm^2, and it is likely that, were they scaled to 1 cm^2 or larger, significantly poorer efficiencies would result due to series resistance issues. Recently, several groups reported improvements in efficiency with single crystal Si microwire arrays.[19−23] Microwire solar cells offer higher open circuit voltages (V_{oc}) than those based on nanowires because, in the latter, the current rapidly saturates, reducing the V_{oc}.[24] A solar cell with arrays of vapor liquid solid (VLS) grown vertical microwire was reported to achieve a conversion efficiency of 7.92%.[19] The device exhibited a V_{oc} of about 0.50 V, a short-circuit current density (J_{sc}) of 24.3 mA/cm^2, and a fill factor (FF) of 65.4%. Among these three parameters, the modest V_{oc} and FF values are the most serious issues, suggesting that the large surface-to-volume

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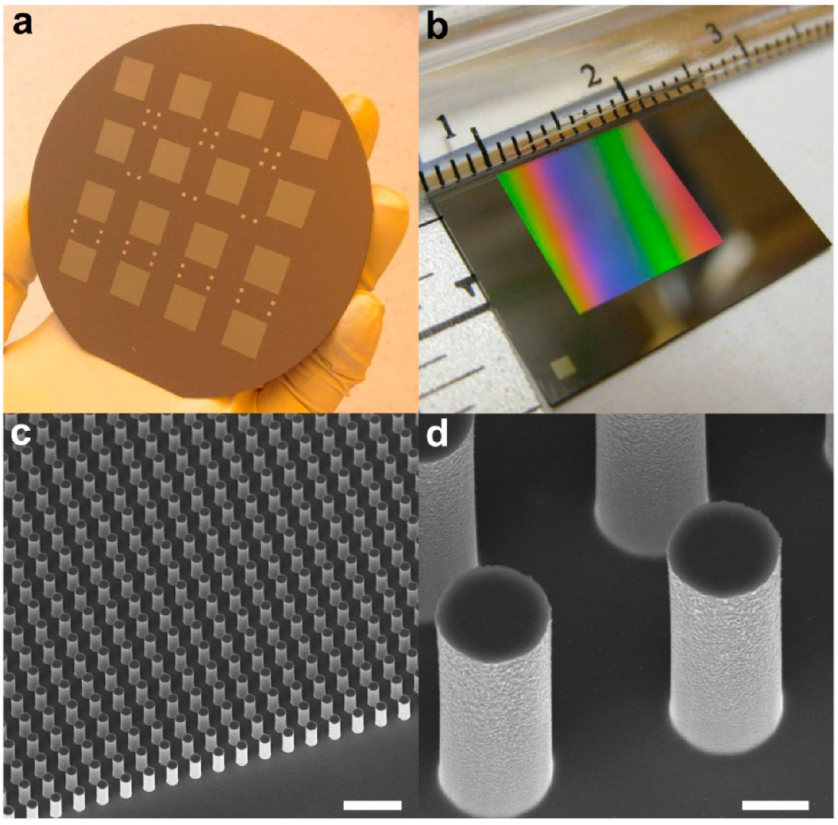

Figure 1. Fabrication of vertical silicon microwire arrays. Optical images of (a) 16 aluminum mask arrays patterned 4-in. Si wafer and (b) dry-etched vertical Si microwire arrays, each having an area of 1 cm^2. (c and d) scanning electron microscope (SEM) images of vertical Si microwire arrays. Scale bars in panels c and d indicate 10 and 1 μm, respectively.

ratios of the wires makes them prone to surface defects and increased series resistance that cause degraded *I*–*V* characteristics and voltage drop, respectively. Here, a microwire Si solar cell is presented with improved performance in V_{oc} and FF. We describe aspects of the design of our devices, and the process by which they are fabricated, and their effects upon the three parameters (V_{oc}, J_{sc} and FF) that determine the overall efficiency of solar cells. Importantly, we show that adding a conformal dielectric layer to the wire surface improves the antireflection performance and therefore the overall solar cell efficiency.

RESULTS AND DISCUSSION

The starting substrate contains a lightly doped p-type epitaxial layer with a resistivity of 11 Ω•cm and a thickness of 22 μm grown on a highly doped handling wafer with a resistivity of 0.01 Ω·cm. In the highly doped handling wafer, the minority carrier diffusion length is about 3 μm.[25] The thickness of the light absorbing region can therefore be taken as 25 μm. This epitaxial Si layer on the handling wafer can be an appropriate platform to mimic the photovoltaic response of ultrathin silicon solar cells.[20] We fabricate an etch mask consisting of an array of aluminum disks using photolithography and liftoff, then form the vertical microwire array by inductively coupled-plasma reactive ion etching (ICP-RIE). As shown in Figure 1a, we fabricate 16 vertical microwire arrays on a 4-in. wafer. Each microwire array is an independent solar cell with an area of 1 cm^2 (Figure 1b). For experimental convenience, we choose the array to be 1 cm^2, although it is scalable up to 4-in. at least, because all the fabrication procedures are carried out on a 4-in. wafer. The diameter, period, and length of the Si microwires are 2, 4, and 6 μm, respectively (Figure 1c,d). In choosing the microwire diameter, we consider the following. If the diameter is too small, *i.e.*, less than 1 μm, the wire with a core–shell p–n junction becomes fully depleted and no neutral region exists. The reduced voltage difference in the junction of the core–shell results in reduced V_{oc}. With this in mind, we choose 2 μm as the diameter.

A highly doped n-type conformal shell for the crystalline p-n junction is formed using the spin-on-doping (SOD) method. After spinning an n-type doping source (P509, Filmtronics, Inc.) on a dummy Si wafer, we position the device wafer containing microwire arrays so that it faces the dummy wafer coated with doping source, and then anneal the pair of wafers at high temperature (900–950 C) for 10 min in a 20% O_2 and 80% N_2 environment. The junction depth is estimated to be 200 nm by diffusion calculations using the program Taurus TSUPREM-4 (Synopsys, Inc.).

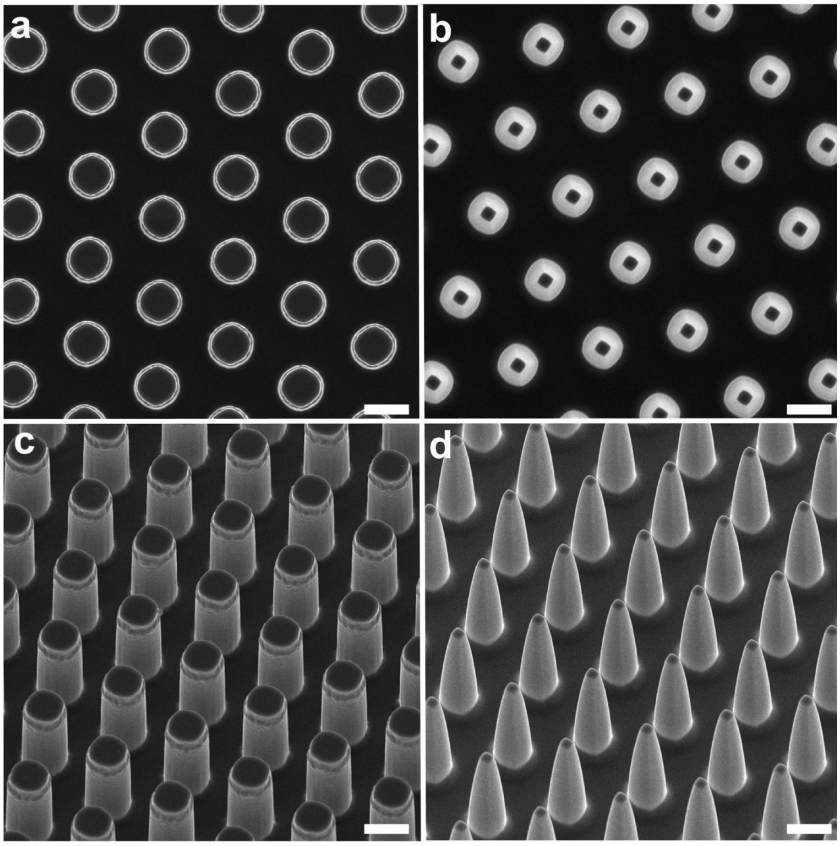

Figure 2. SEM images of vertical Si microwire array after Si wet-etching. Top view (a) and 30° tilted view (c) of microwire arrays after 1 s etching. Top view (b) and 30° tilted view (d) of microwire arrays after 10 s etching. Scale bars indicate 2 μm.

The junction depth plays an important role in determining the device efficiency. The photon absorption in the highly doped n-type shell contributes very little to photocurrent, an effect that is particularly problematic for blue light due to its shorter absorption depth. When annealing time is increased from 10 to 30 min, the measured J_{sc} and overall photovoltaic efficiency reduce by about 41% and 48%, respectively. To construct the top and bottom contacts, aluminum films with thicknesses of 200 nm are deposited on the top and bottom of the wafer using a thermal evaporator. In creating the top contact, the vertical microwire array is covered with positive resist (AZ 40XT, Microchemicals, thickness of 30−100 μm) before the metal deposition using photolithography. The metal therefore serves not only as a contact, but also blocks the light from impinging upon the planar area surrounding the microwire array region (1 cm^2). The photovoltaic properties of our solar cells are characterized under AM 1.5G illumination (Class AAA solar simulator, Sun 3000, Abet Technologies, Inc.).

We next consider methods for mitigating surface imperfections, such as lattice defects and contamination, that could be created by dry etching (Figure 1d).[26−28] Surface damage or contamination could hinder dopant diffusion and result in poor electrical properties at the wire surface. We study two methods for overcoming the problem of surface imperfections: cleaning using piranha, and wet etching. Without cleaning the surface with piranha (at 120 °C for 1 h), the devices show extremely low V_{oc} (<0.5 V) and FF (<55%) which are even lower than those of an earlier study.[19,20] After piranha cleaning, wet etching is performed using isotopic Si etchant (RSE-100, Transene Company, Inc.). As shown in Figure 2, the wet-etched wires are tapered compared to the wires without wet-etching (Figure 1d). Although the etch rate stated by the manufacturer is 2 nm/s at room temperature, the diameter of the top of the wire after 10 s etching (Figure 2d) is only about 500 nm, which is one-quarter of the bare wire diameter. That the etch rate is high could be due to the etching reaction being more vigorous for our wires than for bulk materials, as they have a high surface to volume ratio. This method could be used for fabricating the types of large-scale arrays of highly tapered wires or cones that have been shown offer excellent antireflection properties.[29−31] Our method would have the advantage of being very rapid and not requiring specialized equipment.

Table 1 shows average photovoltaic properties of Si planar and microwire solar cells with and without surface wet-etching. Each entry in this table is the average value, obtained from measurements on four devices. Note that the fabricated microwire solar cells

TABLE 1. Average Photovoltaic Properties of Si Microwire Solar Cells with and without Si Surface Wet-Etching

	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	PCE (%)
Planar solar cell	17.0	0.55	70.7	6.53
Wire solar cell w/o wet-etching	20.5	0.55	72.2	8.07
Wire solar cell w/wet-etching for 10 s	16.7	0.55	73.9	6.85

show a high FF of a maximum of 73.9% which to the best of our knowledge represents the best value among the wire solar cells reported thus far. The V_{oc} is 0.55 V, which is 10% higher than that of a previous study.[19] Furthermore, the J_{sc} values of the wire cells (>20.0 mA/cm^2) are higher than that of the planar device (17.0 mA/cm^2). These values, however, are still lower than those of many commercially available wafer-scale silicon solar cells, for which J_{sc} can exceed 35 mA/cm^2.[2,17,18] We believe that this is due to the absorbing layer of our devices being very thin (~25 μm) compared to those of wafer-scale silicon solar cells (typically several hundred μm thick). Hence, it still remains a great challenge to realize a high J_{sc} device, although various novel approaches have been suggested to improve the trapping efficiency such as adding a mirror layer between the light absorbing layer and the underlying handling wafer.[32] Interestingly, the wet-etched wire solar cell shows only a modest improvement in FF compared to the device without wet-etching. This reveals that piranha cleaning is the most critical step for surface treatment. We also find that the J_{sc} of the wire solar cell is reduced from 20.5 to 16.7 mA/cm^2 after the wet-etching for 10 s. This runs counter to the expectation that the more tapered wire structure would be better for antireflection and would offer higher light absorption due to the gradual transition of the effective optical index from top to bottom of the wire.[5] This is due to the fact that, for the tapered wire structures, the volume of silicon that is photosensitive is smaller. The reflectance at the surface of the tapered wire cell is lower than that of the microwire cell, but this mainly has the effect of increasing the light transmitted to the bottom handling wafer, which does not contribute to the current generation. Based on these results, we choose the wire cell without wet-etching for the experiment we describe next, in which the microwires are coated with a SiO_2 layer.

We next consider the use of a conformal dielectric layer as a means for increasing J_{sc}. This layer bears some similarities to a quarter-wave antireflection coating,[5] but there are also some important differences, as we describe further later. We choose to use SiO_2 for this layer, as measurements on a film on glass reveal it to have much higher optical transmittance (nearly 100% for a 200 nm thick film) than materials such as HfO_2, Al_2O_3, and aluminum-doped zinc oxide (AZO). The SiO_2 layer is deposited by electron cyclotron resonance-plasma enhanced chemical vapor deposition

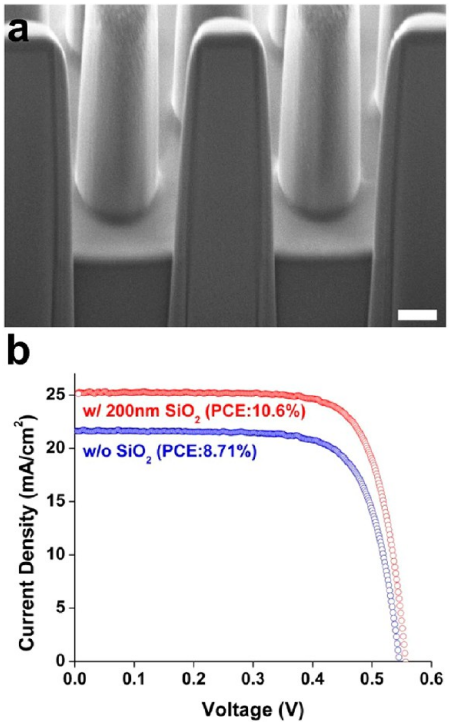

Figure 3. Effect of conformal SiO_2 deposition on wire surfaces. (a) FIB image of cross section of microwires coated with SiO_2. Scale bar indicates 300 nm. (b) Current density–voltage (J–V) characteristics of the Si microwire solar cells, under AM 1.5 G illumination, with and without a 200 nm thick surface SiO_2 coating.

TABLE 2. Average Photovoltaic Properties of Si Microwire Solar Cells with and without Conformal SiO_2 Coating[a]

	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	PCE (%)
w/o SiO_2	20.5 (21.6)	0.55 (0.55)	72.2 (73.7)	8.07 (8.71)
w/200 nm SiO_2	24.1 (25.2)	0.56 (0.56)	72.9 (75.2)	9.73 (10.6)
Improvement (%)	+17.6 (+16.7)	+1.82 (+ 1.82)	+0.97 (+2.04)	+20.6 (+ 21.7)

[a] Values in the brackets are obtained from the champion device.

(ECR-PECVD). These measurements are included in the Supporting Information. Figure 3a shows a focused ion-beam (FIB) cross-section image of silicon wires coated with a thin layer of SiO_2. Although step-coverage of the film deposited by chemical vapor deposition (CVD) is generally not as good as atomic layer deposition (ALD), the deposited film is quite conformal. The optimal thickness of the SiO_2 film is determined by fabricating devices with film thicknesses from 25 to 400 nm, and measuring the photovoltaic properties of each. The deposition of 200 nm films is consistently shown to result in the greatest efficiency improvement (Supporting Information). After the deposition of the 200 nm thick SiO_2 film, the average J_{sc} increases from 20.5 to 24.1 mA/cm^2, representing improvement of 17.6% (Figure 3b and Table 2). Furthermore, the overall average photovoltaic efficiency of the devices reaches 9.73%, representing a 20.6% improvement. As we discuss later, the increase in J_{sc} is found to be consistent

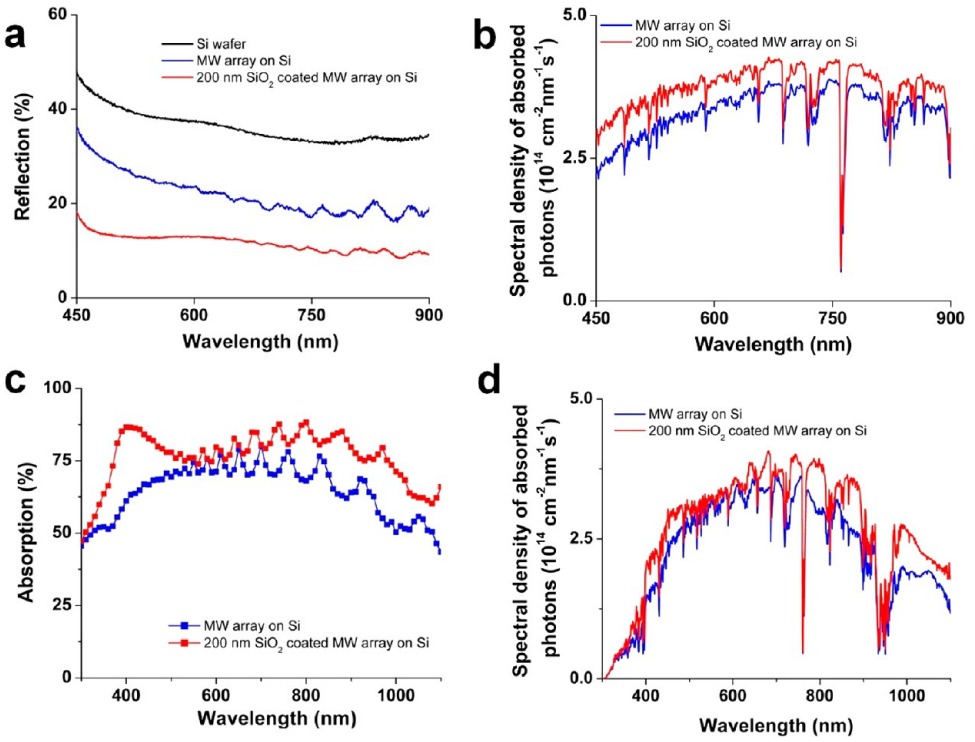

Figure 4. (a) Measured optical reflection spectra from polished Si surface (black line), vertical microwire array on Si surface (blue line), and 200 nm thick SiO_2 coated microwire array on Si surface (red line). (b) Spectral density of absorbed photons under AM1.5G illumination for uncoated Si microwire array (blue line) and coated Si microwire array (200 nm SiO_2, red line) obtained from reflection spectra in panel (a). (c) Simulated (FDTD) absorption spectra of uncoated Si microwire array (blue line) and coated Si microwire array (200 nm SiO_2, red line). (d) Simulated (FDTD) spectral density of absorbed photons under AM1.5G illumination of uncoated Si microwire array (blue line) and coated Si microwire array (200 nm SiO_2, red line).

with the measured reflection spectra and with the predictions of electromagnetic simulations.

We exclude surface passivation effects from being a primary origin of the efficiency improvement because there is no significant difference in efficiency before and after the deposition of a 25 nm thick film (Supporting Information). To clarify the origin of the improved photovoltaic parameters, we measure reflection spectra using a white light illumination setup. Figure 4a shows the reflection spectra of a polished Si surface, a vertical (uncoated) microwire array, and a microwire array coated with a 200 nm thick SiO_2 film. While the polished Si surface shows a reflectance exceeding 35% over a range from 450 to 900 nm, the uncoated microwire array exhibits much reduced reflectance. Furthermore, the reflectance of the coated microwire device drops below 10% at near-infrared wavelengths, which is about half the reflectance of the uncoated microwire device. We next consider the implications of the reduced reflectance on J_{sc}. We use the reflection spectra (Figure 4a) to predict the spectral density of photons absorbed in the silicon. To do this, we take $A(\lambda) = 1 - R(\lambda)$, where $A(\lambda)$ and $R(\lambda)$ are absorption and reflectance, respectively. This is a simplifying assumption, not taking into account transmission and scattering, but permits us to gain physical insight into the mechanism behind the improved performance. We then multiply $A(\lambda)$ by the tabulated AM1.5G illumination spectrum to find the spectral density of photons absorbed in the silicon (Figure 4b). Integrating over the measured wavelength range (450−900 nm) reveals that the total number of absorbed photons is increased by 13.0% with the coated device. We also simulate the absorption in coated and uncoated wires by the finite difference time domain (FDTD) method (Figure 4c). The simulated spectra predict that the absorption is enhanced by the SiO_2 film, with total number of absorbed photons in the 450−900 nm wavelength range being increased by 13.0 %., *i.e.*, in excellent agreement with experiments. We furthermore find that the increase, due to the coating, in the total number of absorbed photons over the complete range of AM1.5G illumination (*i.e.*, 300−1100 nm) is predicted by FDTD to be 16.8%. This is in good agreement with the measured average improvement in J_{sc} of 14 devices, due to the coating, of 17.6% (Table 2). We therefore conclude that our measurements and simulations indicate that the coating improves performance by enhancing absorption. The effect is somewhat similar to that of a quarter-wavelength antireflection coating, with which zero reflectance can be obtained using a film whose refractive index n_{AR} is the geometric mean of the substrate and superstrate. The thickness of such a film should be $d_{AR} = \lambda/(4n_{AR})$. As its refractive index (1.54) is roughly similar to the geometric mean $((n_{Si}n_{air})^{1/2})$ of the

refractive indices of the silicon substrate $n_{Si} = 3.5-5$ and of the air above it ($n_{air} = 1$), SiO_2 could serve as this layer. Calculations, however, reveal that the reflectance from a SiO_2 film (100 nm thick) on flat Si with produces a much lower reflectance than does a 200 nm film. These calculations are presented in the Supporting Information. Hence, we suggest that there may be additional optical phenomena that enhance the light trapping efficiency, for example the SiO_2 layer acting as a cladding to enhance the field confinement in a guided mode of the wire.

CONCLUSION

We have experimentally demonstrated a crystalline microwire solar cell with a power conversion efficiency up to 10.6%. The champion device also exhibits a V_{oc} of 0.56 V, a J_{sc} of 25.2 mA/cm^2, and an extraordinarily high fill factor of 75.2%, despite the photosensitive Si being only 25 μm thick. The high efficiency of the device can be ascribed to the effective antireflection through surface wire patterning and conformal dielectric layer deposition. In particular, the device with 200 nm thick SiO_2 layer shows significant J_{sc} and overall efficiency improvements of 17.6% and 20.6%, respectively. We believe that the wire solar cells would be further improved by optimizing the geometries of the wire arrays and by employing an additional mirror layer beneath the light absorbing layer to reflect the unabsorbed light. The microwire array solar cells with a thin absorber offer opportunities to reduce the surface light reflection and may be useful in the manufacturing of ultrathin highly efficient solar cells with low cost.

METHODS

Microwire Fabrication and Characterization. Vertical silicon microwire arrays are fabricated from a starting Si wafer by dry etching. The starting Si wafer contains a lightly doped p-type epitaxial top layer (11 Ω·cm and 22 μm) grown on a highly doped handling wafer (0.01 Ω·cm and ~500 μm). Microdisk arrays are patterned in LOR3A and Shipley S1805 photoresist using photolithography. After developing the pattern, aluminum is deposited to a thickness of 100 nm and lifted off to leave aluminum microdisk arrays on the starting Si wafer. Inductively coupled plasma-reactive ion etch (STS) is used for anisotropic deep silicon etching at room temperature using the aluminum microdisk arrays as the mask. During this process, 70 sccm of SF_6 and 160 sccm of C_4F_8 gases are used for the etching and surface passivation, respectively. After etching, the aluminum masks are removed using an aluminum etchant—type A (Transene). SEM images are taken on a Zeiss Ultra55.

Solar Cell Fabrication and Power Conversion Efficiency (PCE) Measurements. A highly doped n-type conformal layer on the microwire arrays for the crystalline p—n junction is formed using the spin-on-doping (SOD) method. After spinning an n-type doping source (P509, Filmtronics, Inc.) on a dummy Si wafer, we position the device wafer containing microwire arrays so that it faces the dummy wafer coated with doping source, and then anneal the pair of wafers at high temperature (900—950 C) for 10 min in a 20% O_2 and 80% N_2 environment. To construct the top and bottom contacts, we then thermally evaporate aluminum films with thicknesses of 200 nm on the top and bottom of the wafer. In creating the top contact, the vertical microwire array is covered with positive resist (AZ 40XT, Microchemicals, thickness of 30—100 μm) before the metal deposition using photolithography. The photovoltaic properties of the solar cells are characterized under AM1.5G illumination (Class AAA solar simulator, Sun 3000, Abet Technologies, Inc.).

Reflection Measurements. Reflection measurements are carried out with a white light illumination setup. Light from a fiber-coupled halogen lamp is collimated by an objective lens (magnification, 5×; NA, 0.10), passes through a beam splitter, and is focused by a second objective lens (magnification, 50×; NA, 0.55) onto the microwire array. The reflected light is collected by the same objective lens (50× magnification) and input to a spectrometer equipped with a thermoelectrically cooled CCD array. An iris is used at the image plane of the objective lens to ensure that only the light reflected by the array, and not that from surrounding regions, is detected. The spectra are normalized by the spectrum acquired from a silver mirror (Thorlabs, #PF10-03-P01), thereby enabling the sample reflectance to be found.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Figures of measured optical transmission spectra on AZO, SiO_2, Al_2O_3, and HfO_2 films deposited on glass slide and FDTD simulations of reflection spectra of SiO_2 films of different thicknesses on flat Si substrate; table of photovoltaic properties improvements of Si microwire solar cells after conformal SiO_2 coating. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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